

**AMS-2 DAQ System
JIM-CAN
Hardware Design Specification
(Revised 7)**

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Approval and Signature

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JIM-CAN Flight-Version Board Hardware Design Specification

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1. Overview

1.1 Feature

- 32 bit CompactPCI(CPCI) board compliant with PICMG 2.2 standard
- 32 bit memory mapped address
- Interrupt is provided via PCI bus
- Radiation-Hardened Microcontroller UT69RH051 clocked 11.059 MHz
- Two Intel AN82527 controller clocked with 16 MHz
- Two 256K bytes Dual-Port-RAM(DPRAM)
- Radiation-Hardened UT28F256LV 32K X 8 PROM
- One MAX706 is used to monitor the power status
- Two CAN bus interface according to ISO 11898 physical layer
- One RS232C interface for debug

1.2 Block Diagram

The block diagram of flight version is shown in Figure 1.1. The detailed function description of each block is given in the following sections.

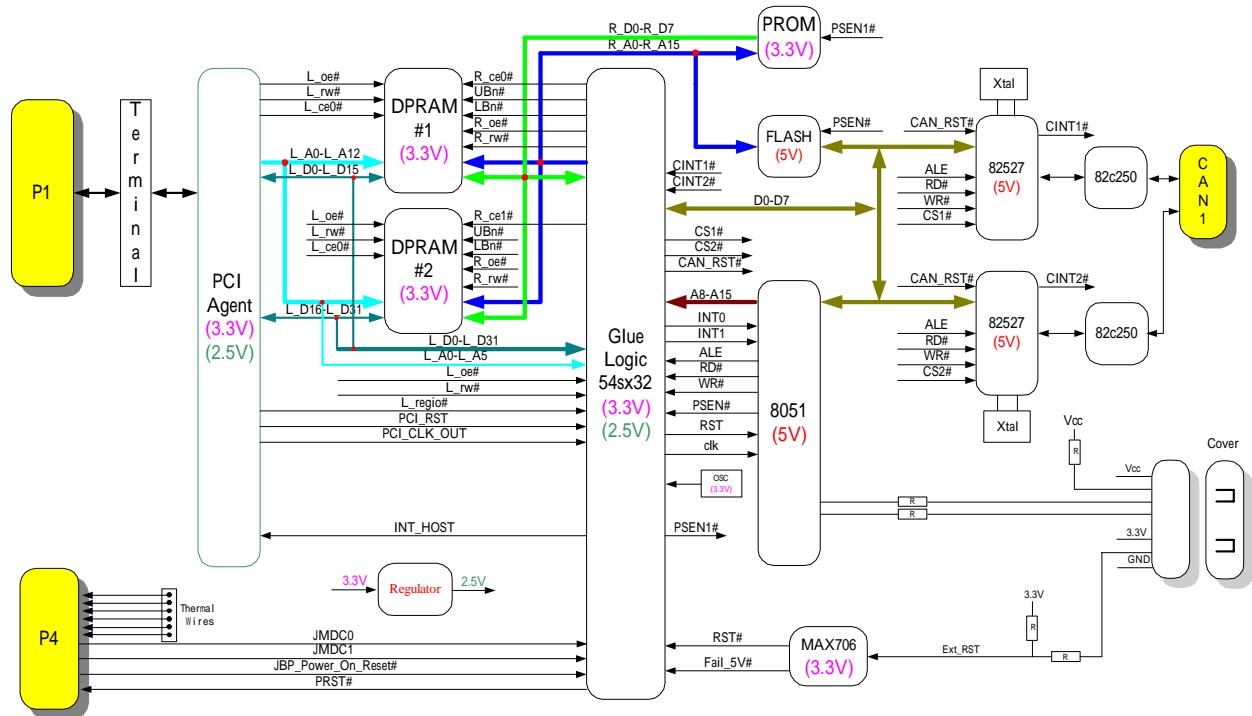


Figure 1.1 Flight version of JIM-CAN Board

1.3 Dual-port RAM

In flight version, two IDT70V28 (64k x 16).dual-port RAM is used as data buffer between JSBC and local *uP* (8051). The DPRAM is divided into several segments to hold data to/from different kind of master/slave node. By this mean, the loading of JSBC could be brought down effectively.

1.4 PCI AGENT

The PCI agent implemented in an anti-fuse FPGA, Actel A54SX, is compliant with PCI 2.2 Specification. The configuration and PCI agent space of PCI agent is shown below:

PCI Configuration Space

Address	Register	Value
CFG-0x00	Vendor ID	0X414D ('AM')
CFG-0x02	Device ID	0X5305 ('S-5')
CFG-0x2C	Sub-Vendor ID	0X4A43 ('JC')
CFG-0x2E	Sub-System ID	0X414E ('AN')
CFG-0x0B	Base-Class Code	0X0C (Serial bus)
CFG-0x0A	Sub-Class Code	0X85
CFG-0x09	Prog. I/F	0X00
CFG-0x08	Rev. ID	0X22 (Rev. 2.2)
CFG-0x10	Base address register #0 of DPM access	By PnP BIOS
CFG-0x14	Base address register #1 of Register access	By PnP BIOS

PCI Agent Space

Address	Register
Dual port memory (DPM) BAR0+0x00000000 ~ BAR0+0x0003FFFF	Dual-port RAM 256KB address space.
BAR1+0x00	Host Control Register (HCR)
BAR1+0x04	Host Status Register 0 (HSR0)
BAR1+0x08	Host Status Register 1 (HSR1)
BAR1+0x0a	Host Error Register (HER)
BAR1+0x10	Interrupt Register for Host (HIE)
BAR1+0x14	Interrupt Register for 8051 (MIE)

For detailed definition of registers, please refer to “JIM-CAN SW Description (V2.0)” by Xu. S.

1.5 Microcontroller

The adoption of 8051 here has several advantages. First, it can reduce the burden of JSBC. Second, when power-up, 8051 can read the Geographic ID (GID) from the board. Third, when 8051 decode a Boot command from CAN bus, it can issue a reset signal to notify JSBC that the reset process must be taken immediately.

1.6 CAN Bus Controller

The Intel AN82527 serial communications controller is a highly integrated device that performs serial communication according to the CAN protocol. The CAN protocol uses a multi-master (contention based) bus configuration for the transfer of ‘communication objects’ between nodes of the network. This multi-master bus is also referred to as CSMA/CR or Carrier Sense, Multiple Access, with Collision Resolution.

The 82527 provides storage for 15 message objects of 8-byte data length. Each message object can be configured as either transmit or receive except for the last message object.

1.7 CAN Bus Driver

The Philips PCA82C250 is the interface between the CAN protocol controller and the physical bus. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller. It is fully compatible with the ISO 11898 standard with data rate up to 1 Mbps.

1.8 PROM

In flight version, one radiation hardened 32K X 8 bit PROM is used to store the program of 8051.

1.9 RS232C

For debugging purpose, the JIM-CAN reserves one RS-232 interface on the board. A external module contains the RS-232 driver can be used to communicate with the monitor program. By this way, we can easily to check whether the JIM-CAN is in a good condition or not.

2. Memory Space

The PC communicates with the board via DPRAM. The memory space of DPRAM is divided into three sections. The first section is local RAM buffer for 8051. The second section is RX/TX buffer for different master/slave nodes. The last section is register area for handshakes for Host CPU and 8051.

2.1 Memory map seen from PCI

In flight version, the memory space on the PC side is 256k bytes. The BAR0 and BAR1, are configuration registers, contain base address for accessing memory and registers. The BAR0 is used for memory access and is assigned by the CPCI PnP Bios. The BAR1 is used for registers access (HCR,HSR0,HSR1,HER,HIE and MIE).

BAR0 Offset	Usage	Real Size
0x00000	8051 RAM Buffer	4 Kbytes
0x1000	Task1 TxBuff	4 Kbytes
0x2000	Task1 RxBuff	4 Kbytes
0x3000	Task2 TxBuff	4 Kbytes
0x4000	Task2 RxBuff	4 Kbytes
0x5000	Task3 TxBuff	4 Kbytes
0x6000	Task3 RxBuff	4 Kbytes
0x7000	Task4 TxBuff	4 Kbytes
0x8000	Task4 RxBuff	4 Kbytes
0x9000	Task5 TxBuff	4 Kbytes
0xA000	Task5 RxBuff	4 Kbytes
0xB000	Task6 TxBuff	4 Kbytes
0xC000	Task6 RxBuff	4 Kbytes
0xD000	Task7 TxBuff	4 Kbytes
0xE000	Task7 RxBuff	4 Kbytes
BAR1 Offset		
0xF000	HCR	4 bytes
0xF004	HSR0	4 bytes
0xF008	HSR1	4 bytes
0xF00C	HER	4 bytes
0xF010	HIE	4 bytes
0xF014	MIE	4 bytes

Notes:

Task definition:

Task	Master	Slave
0		
1	JMDC_M	JMDC_A
2	JMDC_A	JMDC_M
3	JMDC_M	JMDC_B
4	JMDC_B	JMDC_M
5	JMDC_M	JMDC_C
6	JMDC_C	JMDC_M
7	JMDC_M	USCM

* Task 0 is a special task

* Task resource (except task 0)

Including:

2 buffers	(TxBuff, RxBuff)
2 control bits	(TxRqst, RxRqst)
4 status bits	(TxOk, RxOk, Busy, Failed)
4 error bits	(LEC0, LEC1, LEC2, LEC3)
2 can message box	(TxMbox, RxMbox)

Comments:

TxBuff:	Transmit buffer
RxBuff:	Receive buffer
TxRqst:	Transmit request
RxRqst:	Receive request
TxOk:	Transmit a sub-block successfully
RxOk:	Receive a sub-block successfully
Busy:	Task busy
Failed:	Task failed
LEC:	Last error code
TxMbox:	Transmit can message box (according to canid)
RxMbox:	Receive can message box (according to canid)

JMDC ID = 0	A=1	B=2	C=3
JMDC ID = 1	A=0	B=2	C=3
JMDC ID = 2	A=0	B=1	C=3
JMDC ID = 3	A=0	B=1	C=2

2.2 Memory map seen from 8051

Because there maybe at least one masters active in the same time, we must preserve fixed space for holding data to/from the can bus. The default size is 4k bytes each for TX/RX buffer.

Address	Usage	Real Size
0x0000	8051 RAM Buffer	4 Kbytes
0x1000	Task1 TxBuff	4 Kbytes
0x2000	Task1 RxBuff	4 Kbytes
0x3000	Task2 TxBuff	4 Kbytes
0x4000	Task2 RxBuff	4 Kbytes
0x5000	Task3 TxBuff	4 Kbytes
0x6000	Task3 RxBuff	4 Kbytes
0x7000	Task4 TxBuff	4 Kbytes
0x8000	Task4 RxBuff	4 Kbytes
0x9000	Task5 TxBuff	4 Kbytes
0xA000	Task5 RxBuff	4 Kbytes
0xB000	Task6 TxBuff	4 Kbytes
0xC000	Task6 RxBuff	4 Kbytes
0xD000	Task7 TxBuff	4 Kbytes
0xE000	Task7 RxBuff	4 Kbytes
0xF000	HCR	4 bytes
0xF004	HSR0	4 bytes
0xF008	HSR1	4 bytes
0xF00C	HER	4 bytes
0xF010	HIE	4 bytes
0xF014	MIE	4 bytes
0xF100	CAN Controller 1	256 bytes
0xF200	CAN Controller 2	256 bytes

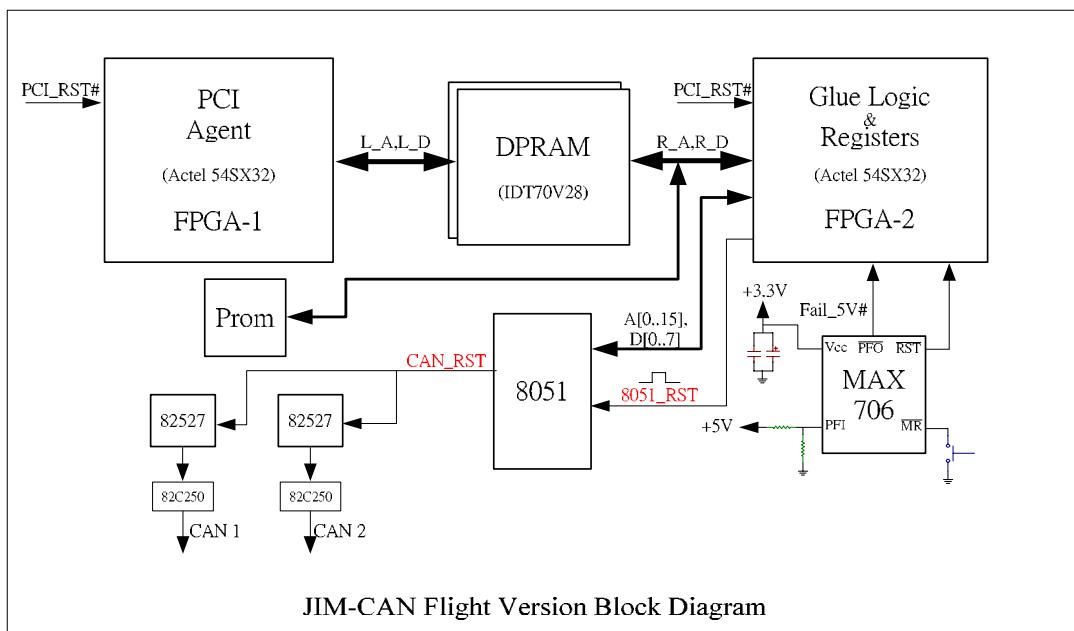
2.3 CAN controller

Two Can controllers are installed on JIM-CAN. They are accessed with CS1 and CS2 signals. The 1st CAN controller is mapped in the memory area from 0xf100h to 0xf1FFh, the 2nd CAN controller is mapped in the memory area from 0xf200h to 0xf2FFh of 8051. With an access to the memory area the corresponding CAN controller is automatically selected. The detailed register description can be found in the data sheet.

Both CAN controllers are clocked with 16 MHz. A low-level signal comes from the FPGA resets the CAN controllers.

CAN Controller	Base Address	Interrupt at 8051	Hardware Reset
1st CAN Controller	0xf100h	Int0	FPGA
2nd CAN Controller	0xf200h	Int1	FPGA

3. Board Initialization Process



JIM-CAN Board Initialization Process

	FPGA-1,FPGA-2	Other components
(1) Local Power-On	<ul style="list-style-type: none"> (a) When power on, the PCI Agent (FPGA-1) will enter its initial state. (b) The registers (Control/Status/Error /Command) in FPGA-2 will be set to the default values. 	<ul style="list-style-type: none"> (a) When power on, every chip will enter into its initial state. (b) The MAX706 will assert RST# to FPGA-2, which generates 8051_RST signal to reset 8051. (c) The Max706 also can monitor +3.3V and +5V. If the any voltage falls below its threshold, then a reset signal will send to FPGA-2. The FPGA-2 generates the 8051_RST signal to 8051. (d) 8051 will do the reset procedures (see item 3).
(2) PCI_RST#	<ul style="list-style-type: none"> (a) PCI_RST# will reset the PCI Agent (FPGA-1). (b) The JSBC_WAS_RESET bit, in FPGA-2, will be asserted when PCI_RST# occurs. This bit can only be read and clear by the 8051. (c) The registers in FPGA-2 should retain its states. 	<ul style="list-style-type: none"> (a) The PCI_RST# does not disturb the 8051. The status bit, JSBC_WAS_RESET, in FPGA-2 can be observed by that the 8051. (b) Other peripherals are not affected by PCI_RST#.
(3) Command Reset by JSBC	<ul style="list-style-type: none"> (a) This command is the software reset by JSBC. 	<ul style="list-style-type: none"> 8051 reset procedures: <ul style="list-style-type: none"> (a) 8051 Initials local variables. (b) 8051 resets CAN controllers. (c) 8051 initializes CAN controllers to the default values defined in JIM-CAN Protocol. (d) 8051 Clears the contents of DPRAM and sets the default values of registers in FPGA-2.

4. Configurations

4.1 Program Source

The following figure 3-1 shows a diagram of JIM-CAN board. The program for 8051 is either on the flash memory or PROM. When using flash memory, a 0 Ohm (R17) must be mounted. If PROM is adopted then a 0 Ohm (R18) will be mounted.

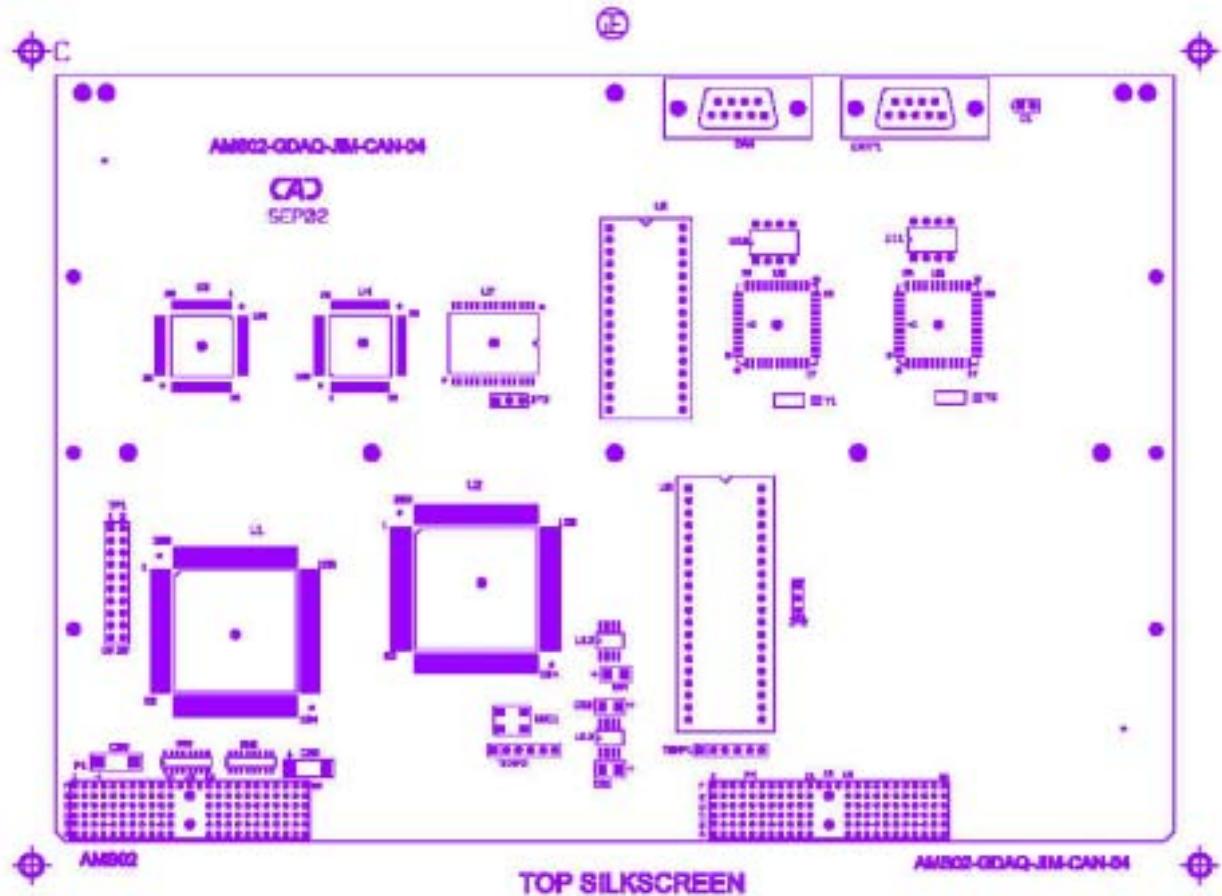


Figure 3.1 Components placement

4.2 Dallas Sensors

There are two groups of Dallas temperature sensors (Temp1 and Temp2) reserved on the board. The sensors are used to monitor the temperature of JIM-CAN board.

4.3 Pin assignment

4.3.1 CAN bus and RS232C interface

CAN bus interface		RS232C interface	
Pin No.	Signal	Pin No.	Signal
1	CAN A-	1	+5V
2	CAN A+	2	
3	CAN B-	3	RxD
4	CAN B+	4	TxD
5	GND	5	+3.3V
6	GND	6	Button RST
7	GND	7	GND
8	GND	8	
9	Shield	9	

5. Power Issue

In flight version, only one regulator will be adopted to provide + 2.5V for PCI agent and the +3.3V source will be supplied from CPCI bus.

The total power consumption is estimated as follow:

Voltage	Current	Total Power Consumption	# of DC/DC	Latch-up Protection
+5V	0.35A (Typical) 0.42 A (Max)	3.07 W (Typical) 3.684 W (Max)	+3.3V → +2.5V	None
+3.3V	0.40A (Typical) 0.48A (Max)			

6. Backplane Assignment

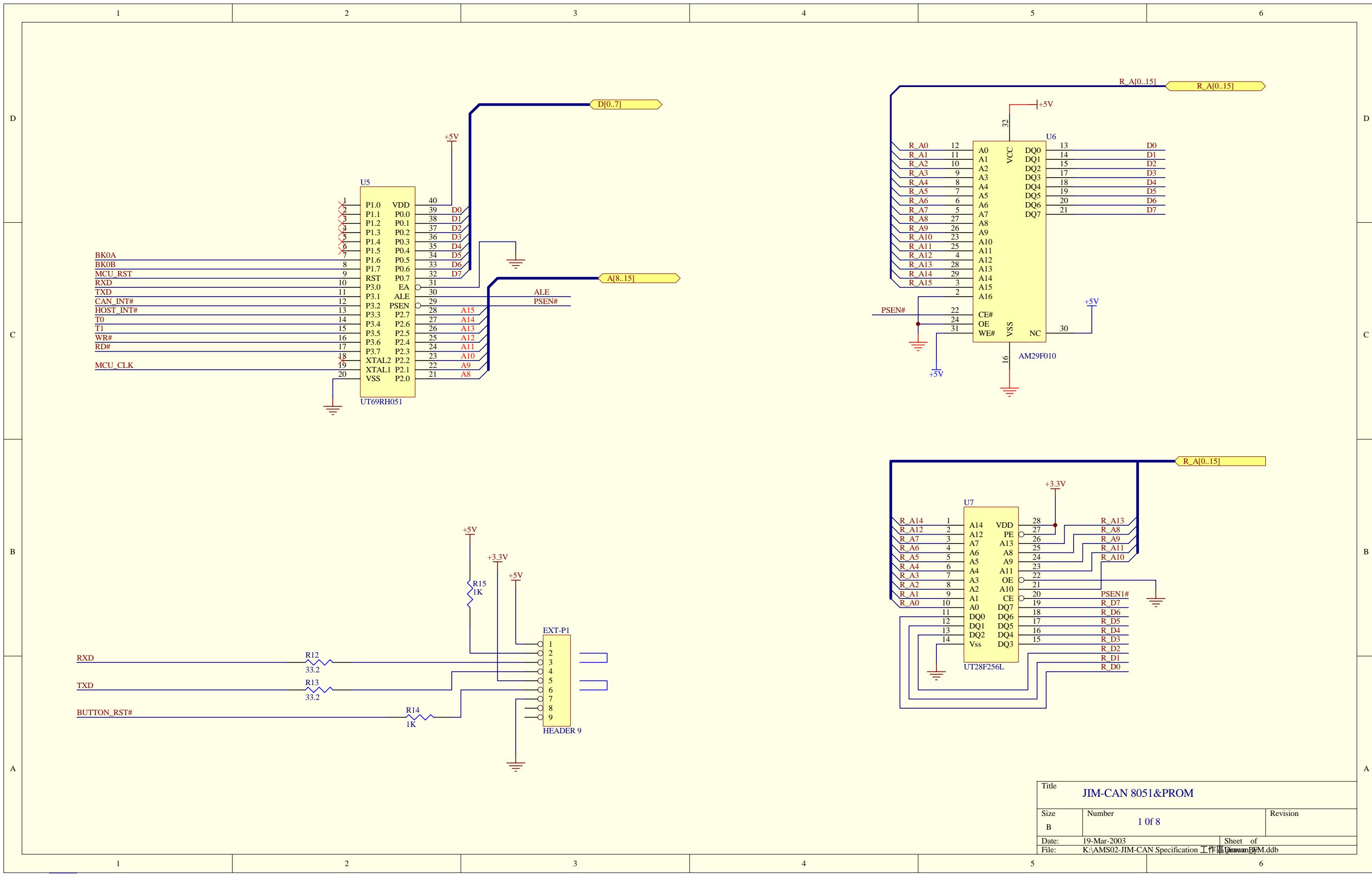
P1 for JIM-CAN Peripheral Slot Connector Pin Assignments:

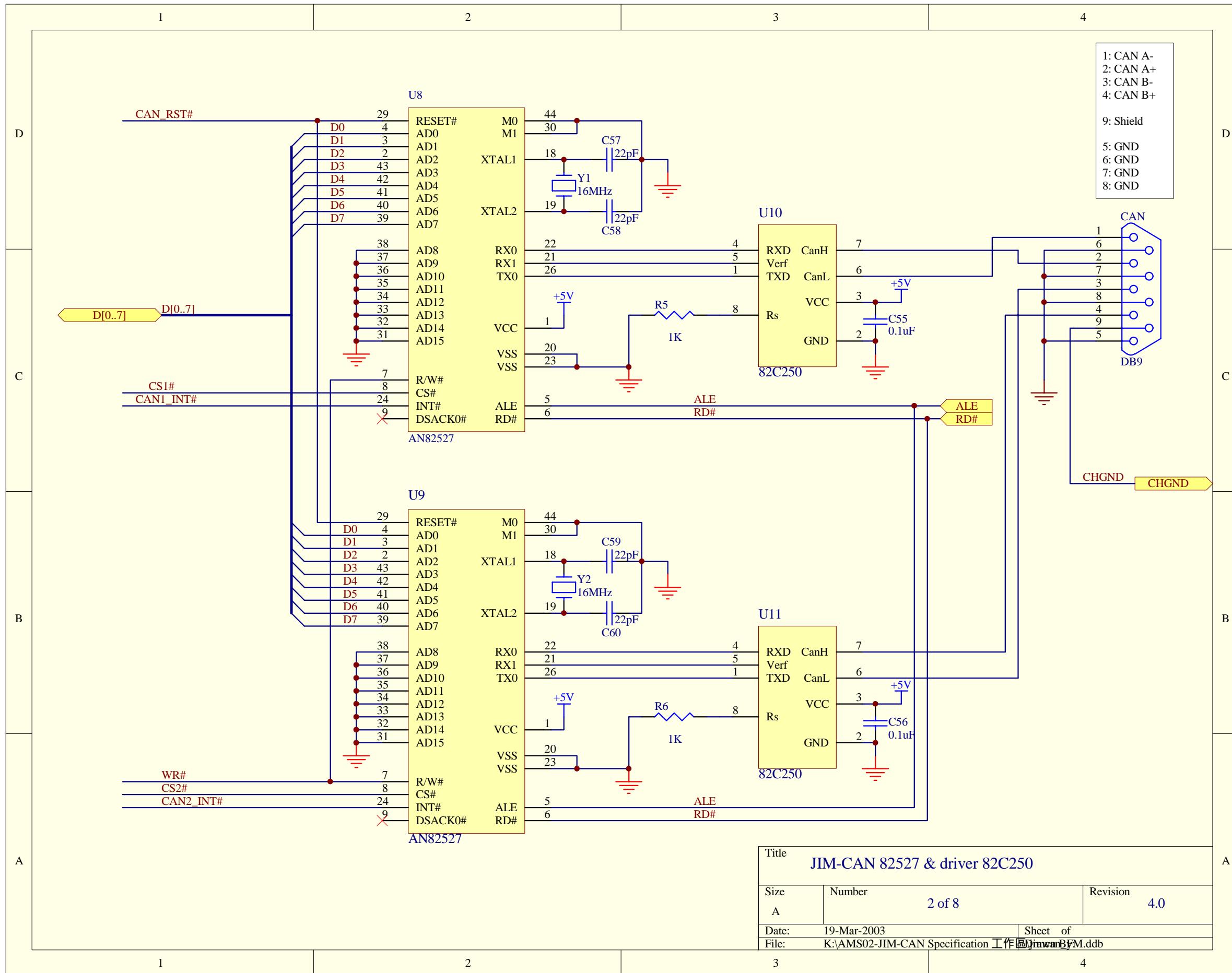
	Pin	Z	A	B	C	D	E	F
P1 C O N N E C T O R	25	GND	5V	REQ64#	GND	3.3V	5V	GND
	24	GND	AD[1]	5V	3.3V	AD[0]	ACK64#	GND
	23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
	22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
	21	GND	3.3V	AD[9]	AD[8]	GND	C/BE[0]#	GND
	20	GND	AD[12]	GND	3.3V	AD[11]	AD[10]	GND
	19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
	18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
	17	GND	3.3V	GND	GND	GND	PERR#	GND
	16	GND	DEVSEL#	GND	3.3V	STOP#	LOCK#	GND
	15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
	12-14	GND	KEY AREA					GND
	11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
	10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
	9	GND	C/BE[3]#	AD[31]	AD[23]	GND	AD[22]	GND
	8	GND	AD[26]	GND	3.3V	AD[25]	AD[24]	GND
	7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
	6	GND	REQ0#	GND	3.3V	CLK1	AD[31]	GND
	5	GND	GND	GND	RST#	GND	GNT0#	GND
	4	GND	GND	GND	3.3V	GND	GND	GND
	3	GND	INTD#	INTA#	INTB#	5V	INTC#	GND
	2	GND	GND	5V	GND	GND	GND	GND
	1	GND	5V	-12V	GND	+12V	5V	GND
	Pin	Z	A	B	C	D	E	F

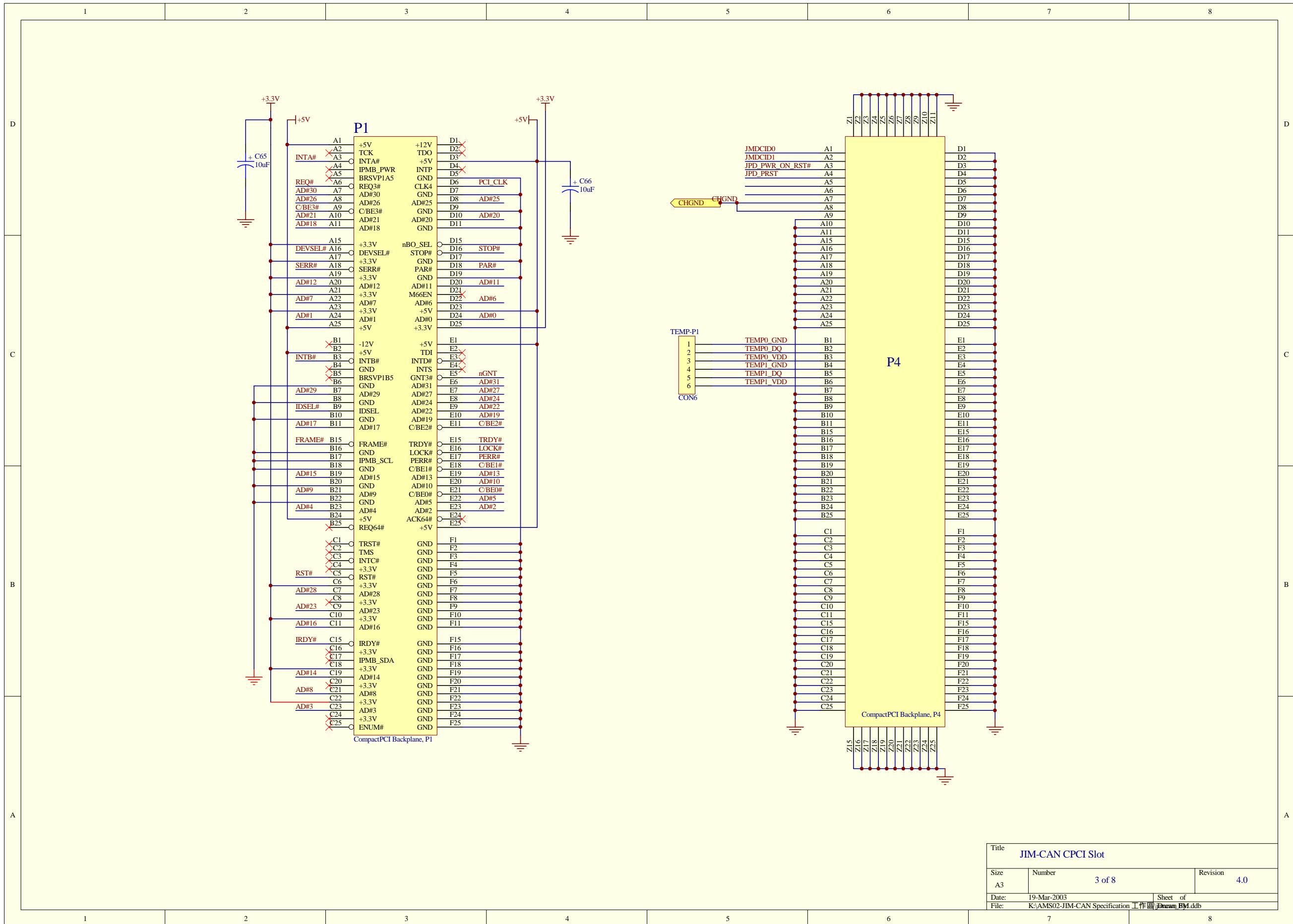
P4 for JIM-CAN Connector Pin Assignments:

	Pin	Z	A	B	C	D	E	F
P4 C O N N E C T O R	25	GND	GND	GND	GND	GND	GND	GND
	24	GND	GND	GND	GND	GND	GND	GND
	23	GND	GND	GND	GND	GND	GND	GND
	22	GND	GND	GND	GND	GND	GND	GND
	21	GND	GND	GND	GND	GND	GND	GND
	20	GND	GND	GND	GND	GND	GND	GND
	19	GND	GND	GND	GND	GND	GND	GND
	18	GND	GND	GND	GND	GND	GND	GND
	17	GND	GND	GND	GND	GND	GND	GND
	16	GND	GND	GND	GND	GND	GND	GND
	15	GND	GND	GND	GND	GND	GND	GND
	12-14	KEY AREA						
	11	GND	GND	GND	GND	GND	GND	GND
	10	GND	GND	GND	GND	GND	GND	GND
	9	GND	GND	GND	GND	GND	GND	GND
	8	GND	CHGND	GND	GND	GND	GND	GND
	7	GND	CHGND	GND	GND	GND	GND	GND
	6	GND	GND	TEMP1_VDD	GND	GND	GND	GND
	5	GND	GND	TEMP1_DQ	GND	GND	GND	GND
	4	GND	JPB_PRST	TEMP1_GND	GND	GND	GND	GND
	3	GND	JPB_PWR_ON_RST#	TEMP0_VDD	GND	GND	GND	GND
	2	GND	MDCID[1]	TEMP0_DQ	GND	GND	GND	GND
	1	GND	MDCID[0]	TEMP0_GND	GND	GND	GND	GND
	Pin	Z	A	B	C	D	E	F

7. Schematic







2002/7/24

數量	Part No.	位置	包裝	說明
2	A54SX32A-3PQ208I	U1 U2	PQFP-208	Actel FPGA A54SX16A, A54SX32A and A54SX72A
2	IDT70V28L15PFI	U3 U4	TQFP-100	Cypress Dual-port SRAM 64K x 16
1	5962H9563801VQA	U5	DIP-40	UTMC UT69RH051
1	AM29F010	U6	DIP-32	Flash Memory
1	5962H0151701QXA	U7	FP-28	UTMC PROM 32K X 8
2	AN82527F8	U8 U9	PLCC-44	Intel CAN Protocol Controller
2	PCA82C250N	U10 U11	DIP-8	Philips CAN Bus Driver
1	LP2989AIM	U12	SO-8	2.5V Voltage Regulator
1	MAX706SESA	U13	SO-8	+3V Voltage Monitoring, Low-Cost, Supervisory Circuit
2	CX-2-02-16MHz	Y1 Y2	PTB-2	Crystal
1	CXO3M-10N-SM3-11.059MHz	OSC1	LCC-4	Oscillator
2	M83513/03-A11N	EXT-P1 ,CAN	Micro-D	Micro D, Flying Lead, (Insert Materials A or B)
2	1721 110 2102	P1 P4	CON132	Backplane, J1 and J4, 110 Positions
2	M55342K06B10D0S	R10 R16	C0805	10
2	M55342K06B33D2S	R12 R13	C0805	33.2
1	M55342K06B787DS	R18	C0805	787
4	D55342K07B1E00S	R5 R6 R14 R15	C1206	1K
1	M55342K06B1E30S	R17	C0805	1.3K
1	M55342K06B10E5S	R8	C0805	10.5K
1	M55342K06B28E0S	R7	C0805	28K
1	M55342K06B100ES	R9	C0805	100K
1	D55342K07B330ES	R19	C1206	330K
6	M914D05K10R0FAM	RN1 RN2 RN3 RN4 RN5 RN6	C4115	16-PIN Network Resister
4	CDR31BP220BKUS	C57 C58 C59 C60	C0805	22pF
1	CDR31BX103AKUS	C62	C0805	0.01uF

2002/7/24

數量	Part No.	位 置	包 裝	說	明
56	1206B104K101KYHT	C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C43 C44 C45 C46 C47 C48 C49 C50 C51 C52 C53 C54 C55 C56	C1206	0.1uF	
1	CWR11JH225KC	C61	C3528	2.2uF	
1	CWR11FH475KC	C63	C3528	4.7uF	
1	CWR11FH685KC	C64	C3528	6.8uF	
4	CWR11KH106KC	C65 C66 C69 C70	C7343	10uF	

